



HITACHI

KAOHSIUNG HITACHI ELECTRONICS CO., LTD.

FOR MESSRS: _____

DATE: Oct. 3th 2011

TECHNICAL DATA

TX31D38VM2BAA

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2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 12.3" HSXGA of 8:3 format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX31D38VM2BAA
Module Dimensions	320(W) mm x 130(H) mm x (12.8)(D) mm typ.
LCD Active Area	293.76(W) mm x 110.16(H) mm
Pixel Pitch	0.2295(W) mm x 0.2295(H) mm
Resolution	1280 x 3(RGB)(W) x 480(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color TFT; Normally White
Display Type	Active Matrix
Number of Colors	262k Colors
Backlight	LED (Lifetime: 70 Khrs)
Weight	(606) typ. (g)
Interface	LVDS; 20 pins
Power Supply Voltage	3.3V for LCD; 12V for Backlight
Power Consumption	(T.B.D)W for LCD; (T.B.D)W for backlight
Viewing Direction	12 o'clock (The direction without image inversion and least brightness change)



4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	VDD	0	4.0	V	-
Input Voltage of Logic	VI	-0.3	VDD+0.3	V	Note 1
Operating Temperature	Top	-30	80	°C	Note 2
Storage Temperature	Tst	-40	90	°C	Note 2
Backlight Input Voltage	VLED	-	15	V	Note 3

Note 1: It shall be applied to pixel data signal, clock signal and control Pin.

Note 2: The maximum rating is defined as above based on the temperature on the panel surface, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.

Note 3: Do not operate at or near the maximum rating listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

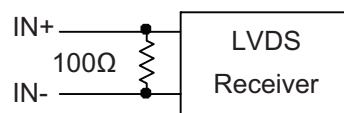
 $T_a = 25\text{ }^{\circ}\text{C}$, $V_{SS} = 0\text{V}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	VDD	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	VI	VIH	-	-	+100	mV	Note 1
		VIL	-100	-	-		
Power Supply Current	IDD	VDD-VSS =3.3V	-	(580)	-	mA	Note 2,3
Vsync Frequency	f_v	-	-	60	T.B.D	Hz	Note 4
Hsync Frequency	f_H	-	-	31.8	T.B.D	KHz	
DCLK Frequency	f_{CLK}	-	-	43.2	T.B.D	MHz	

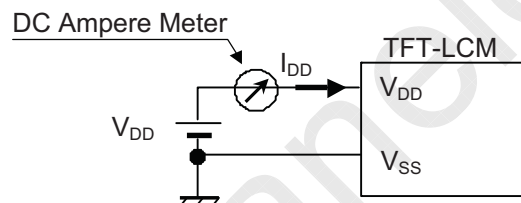
Note 1: VCM=+1.2V

VCM is common mode voltage of LVDS transmitter/receiver.

The input terminal of LVDS transmitter is terminated with 100Ω.



Note 2: An all black check pattern is used when measuring IDD, f_v is set to 60Hz.



Note 3: 1.0A fuse is applied in the module for IDD. For display activation and protection purpose, power supply is recommended larger than 2.5A to start the display and break fuse once any short circuit occurred.

Note 4: For LVDS transmitter input.

Note 5: Vertical Frequency is encouraged to be used by 60Hz.

5.2 BACKLIGHT CHARACTERISTICS

 $T_a = 25\text{ }^{\circ}\text{C}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	VLED	-	-	12	-	V	Note1
LED Forward Current (Dim Control)	ILED	0V; 0% duty	-	T.B.D	-	mA	Note 2
		3.3VDC; 100% duty	-	T.B.D	-		
LED lifetime	-	(T.B.D) mA	-	70K	-	hrs	Note 3

Note 1: As Fig. 5.1 shown, LED current is constant, (T.B.D)mA, controlled by the LED driver when applying 12V VLED.

Note 2: Dimming function can be obtained by applying DC voltage or PWM signal from the display interface CN1. The recommended PWM signal is 1K ~ 10K Hz with 3.3V amplitude.

Note 3: The estimated lifetime is specified as the time to reduce 50% brightness by applying (T.B.D)mA at 25°C.

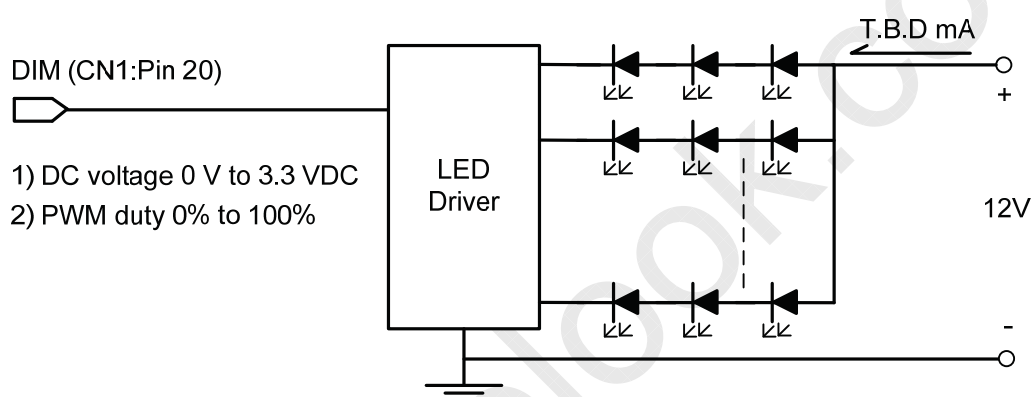


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25°C.
- In the dark room around 500~1000 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$$T_a = 25^{\circ}\text{C}, f_v = 60\text{ Hz}, VDD = 3.3\text{V}$$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$, ILED= (T.B.D) mA	800	1000	-	cd/m ²	Note 1
Brightness Uniformity		-		70	-	-	%	Note 2
Contrast Ratio		CR		640	800	-	-	Note 3
Response Time (Rising + Falling)		T _r + T _f	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	25	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	60	-	%	-
Viewing Angle		θ_x	$\phi = 0^{\circ}, CR \geq 10$	60	80	-	Degree	Note 5
		$\theta_{x'}$	$\phi = 180^{\circ}, CR \geq 10$	60	80	-		
		θ_y	$\phi = 90^{\circ}, CR \geq 10$	50	60	-		
		$\theta_{y'}$	$\phi = 270^{\circ}, CR \geq 10$	70	80	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	(0.60)	-	-	Note 6
		Y		-	(0.35)	-		
	Green	X		-	(0.34)	-		
		Y		-	(0.60)	-		
	Blue	X		-	(0.14)	-		
		Y		-	(0.11)	-		
	White	X		-	(0.30)	-		
		Y		-	(0.35)	-		

Note 1: The brightness is measured from center point of the panel, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

, which is based on the brightness values of the 9 points measured by BM-5 as shown in Fig. 6.2.

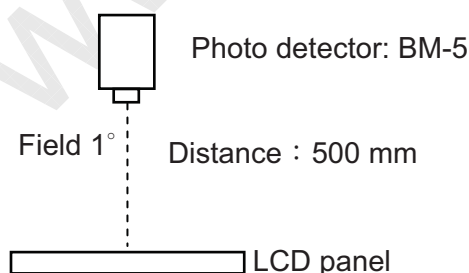


Fig. 6.1

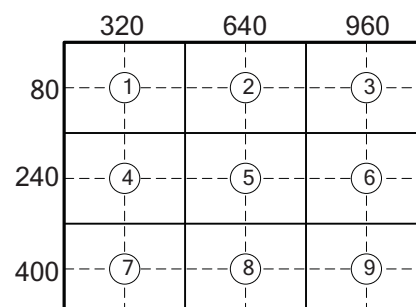


Fig. 6.2

Note 3: The contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 90% brightness to 10% brightness when the data is from white to black. Oppositely, Falling time is the period from 10% brightness rising to 90% brightness.

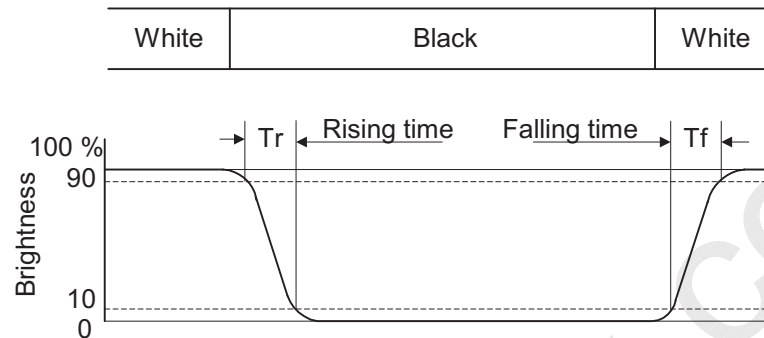


Fig. 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The viewing direction of this display is 12 o'clock, which means that a photograph with gray scale would not be reversed in color and the brightness change would be less from this direction. However, the best contrast peak would be located at 6 o'clock.

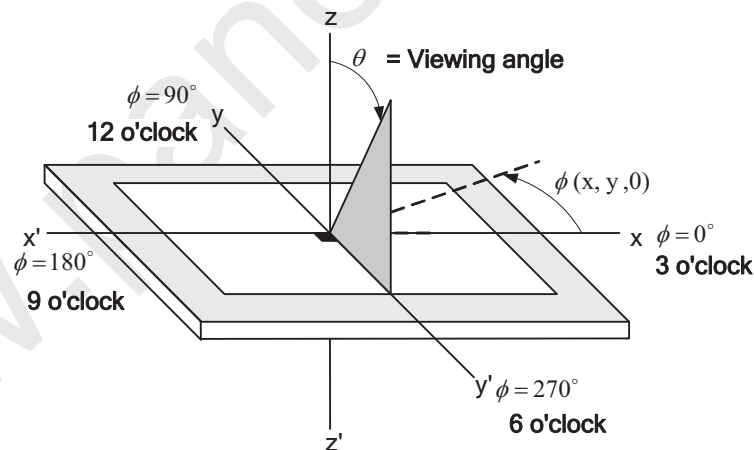
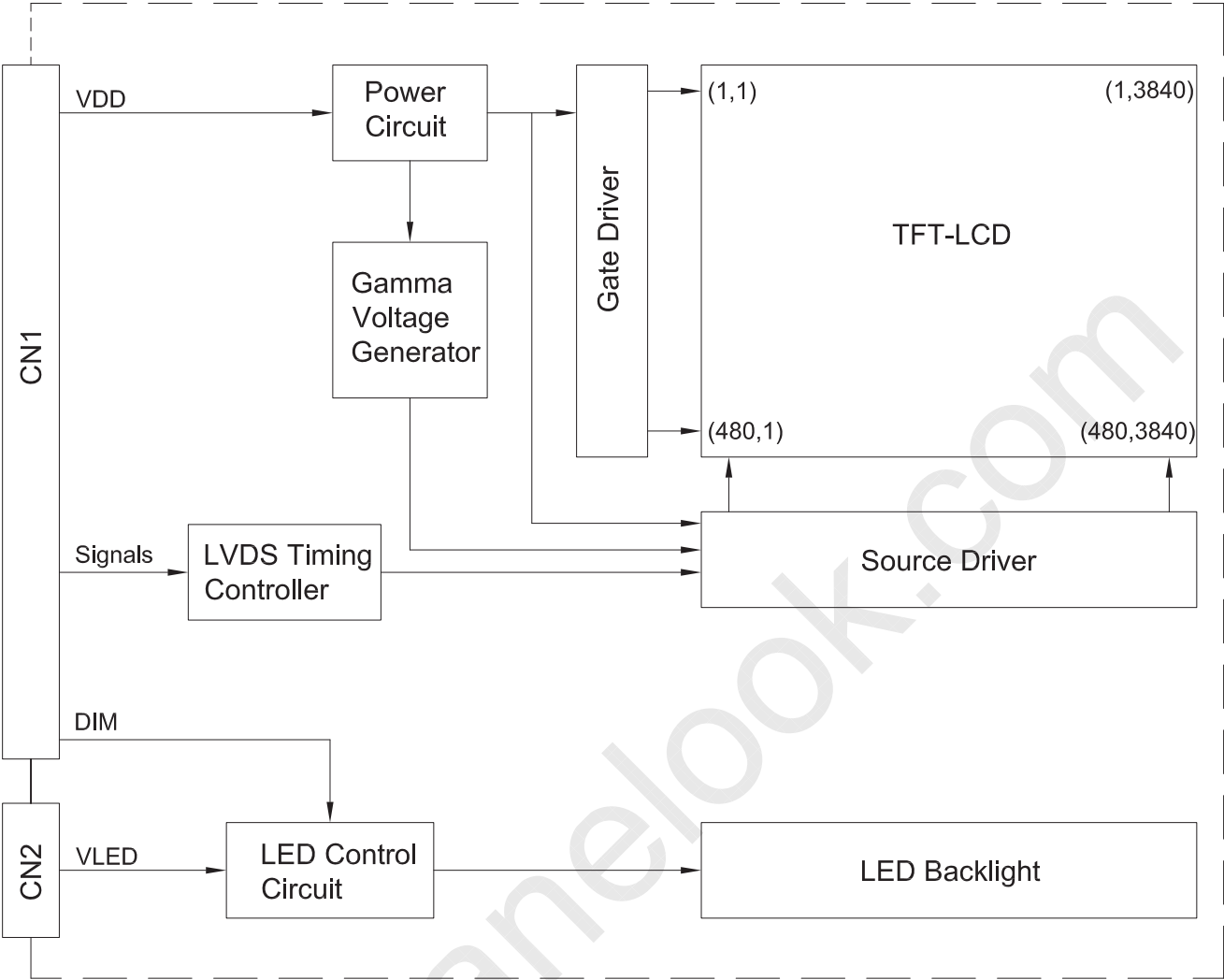


Fig. 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7 BLOCK DIAGRAM



Note: Signals are CLK, and pixel data pairs.

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8. LCD INTERFACE

8.1 INTERFACE PIN CONNECTIONS

The display interface connector (CN1) is FI-SEB20P-HF13E made by JAE and pin assignment is as below:

Pin No.	Symbol	Signal
1	VDD	Power Supply for Logic
2	VDD	
3	VSS	GND
4	VSS	
5	IN0-	R0~R5, G0
6	IN0+	
7	VSS	GND
8	IN1-	G1~G5, B0~B1
9	IN1+	
10	VSS	GND
11	IN2-	B2~B5, DE
12	IN2+	
13	VSS	GND
14	CLK IN-	Pixel Clock
15	CLK IN+	
16	VSS	GND
17	NC	No Connection
18	NC	
19	VSS	GND
20	DIM	Normal Brightness: 0V or 0% PWM Duty Brightness Control: 0V to 3.3 VDC or 0% to 100% PWM Duty

Note 1: IN n- and IN n+ (n=0, 1, 2), CLK IN- and CLK IN+ should be wired by twist-pairs or side-by-side FPC patterns, respectively.

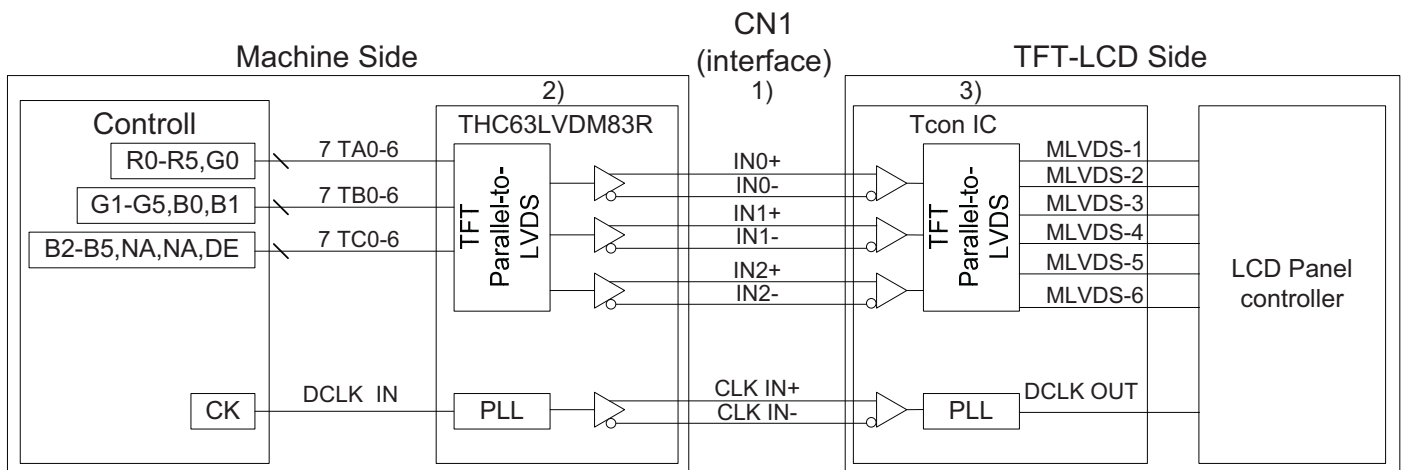
Note 2: All VSS pins should be connected to GND(0V), Metal bezel is connected internally to VSS.

Note 3: Normal brightness: 0V or 0% PWM duty; Brightness Control: 0V to 3.3V DC or 0% to 100% PWN duty.

The backlight connector (CN2) is SM02(8.0)B-BHS-1-TB (LF)(SN) made by JST, and pin assignment is as below:

Pin No.	Symbol	Signal
1	VLED	12VDC
2	GND	Ground

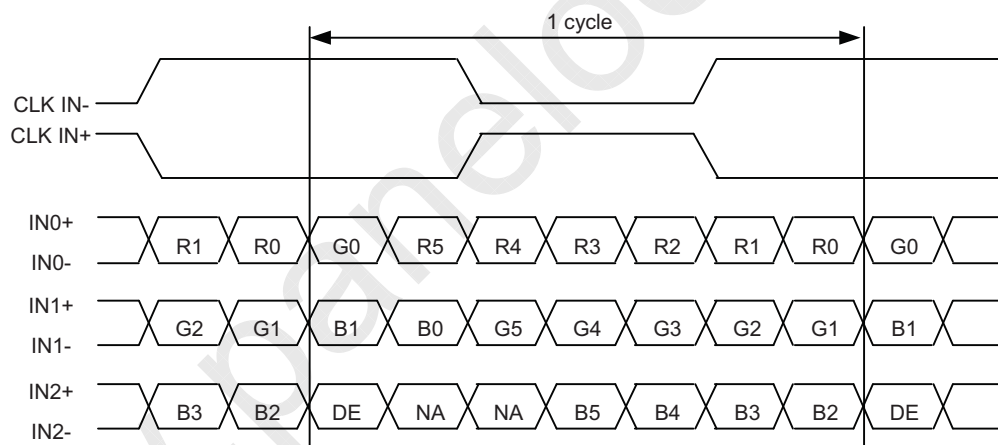
8.2 LVDS INTERFACE



Note 1: LVDS cable impedance should be 100 ohms per signal line when each 2-lines (+, -) is used in differential mode.

Note 2: The recommended transmitter, THC63LVDM83R, is made by Thine or equivalent, which is not contained in the module.

8.3 LVDS DATA FORMAT



DE: Display Enable

NA: Not Available

8.4 INTERFACE TIMING SPECIFICATIONS

The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (Vsync) = 60 Hz to define. If 60 Hz is not the aim to set, less than 66 Hz for Vsync is recommended to apply for better performance by other parameter combination as the definitions in section 5.1.

Item		Symbol	Min.	Typ.	Max.	Unit
DCLK	Cycle frequency	$1/t_{CLK}$	T.B.D	43.2	T.B.D	MHz
	Low level width	t_{WCL}	10	-	-	ns
	High level width	t_{WCH}	10	-	-	
	Rise / Fall time	t_{rCLK}, t_{fCLK}	-	-	12	
	Duty	D	0.4	0.5	0.6	-
DTMG	Set up time	t_{SI}	8	-	-	ns
	Hold time	t_{HI}	8	-	-	
	Rise / Fall time	t_{r}, t_{f}	-	-	12	ns
	Horizontal cycle	t_H	T.B.D	1360	T.B.D	t_{CLK}
	Horizontal valid data width	t_{HD}	1280	1280	1280	
	Horizontal porch width	t_{HB}	T.B.D	80	T.B.D	
	Vertical cycle	t_V	T.B.D	530	T.B.D	t_H
	Vertical valid data width	t_{VD}	480	480	480	
	Vertical porch width	t_{VB}	T.B.D	50	T.B.D	
Data	Set up time	t_{SD}	8	-	-	ns
	Hold time	t_{HD}	8	-	-	
	Rise / Fall time	t_{Dr}, t_{Df}	-	-	12	ns

8.5 TIMING CHART

DTMG (Data Enable) is the signal to determine valid data, and the timing of DTMG can be determined from Hsync and Vsync as below. For this display, only DTMG and DCLK are the essential signals. Hsync and Vsync are not necessary to connect to display interface after DTMG has been generated and input.

DE MODE

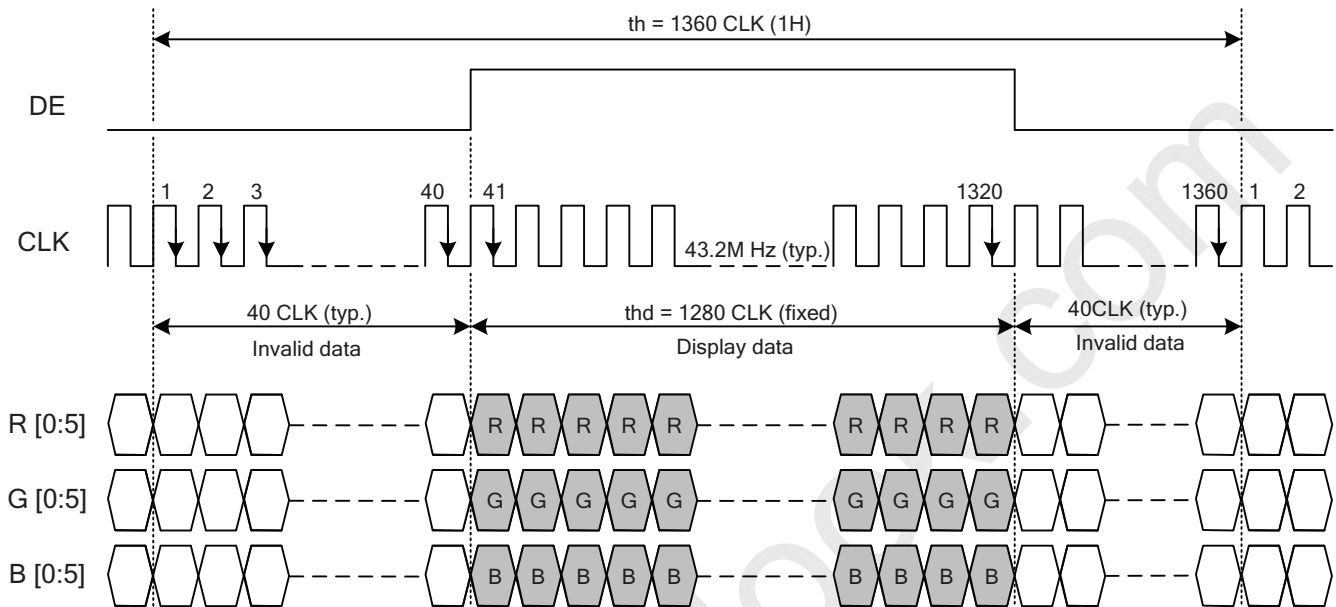


Fig. 8.3 Horizontal Timing of DE Mode

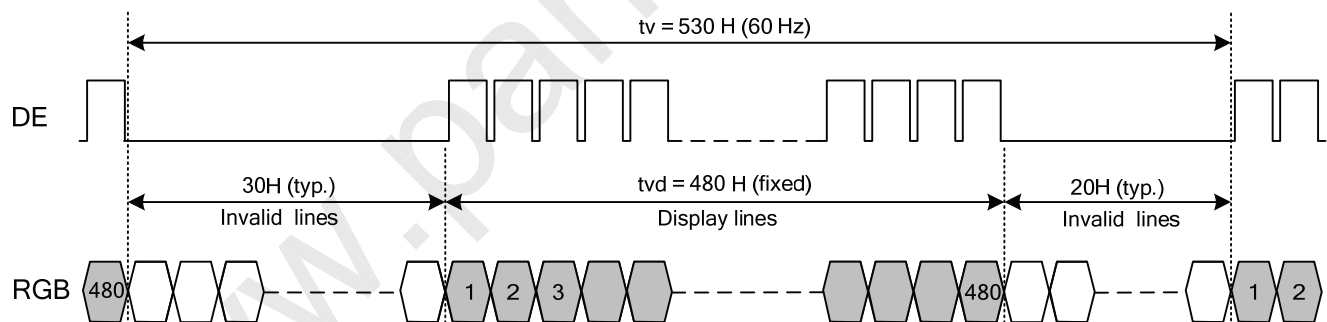
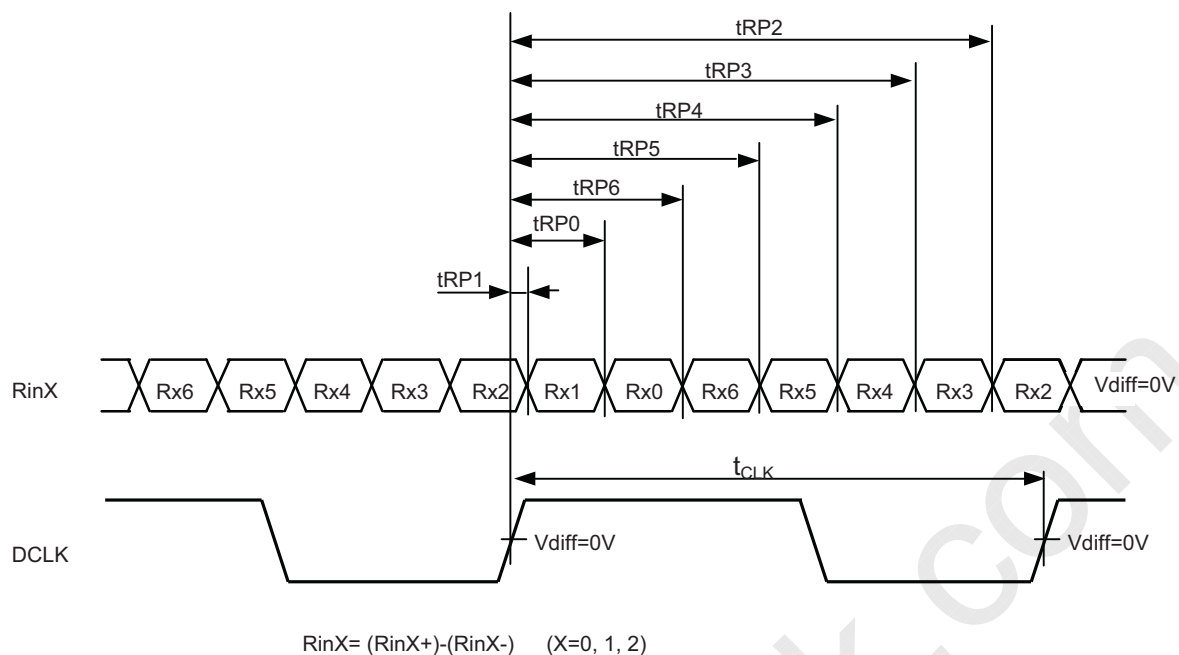


Fig. 8.4 Vertical Timing of DE Mode

8.6 LVDS RECEIVER TIMING



Item		Symbol	Min.	Typ.	Max.	Unit
DCLK	Frequency	$1/t_{CLK}$	T.B.D	43.2	T.B.D	MHz
RinX (X=0,1,2)	0 data position	t_{RP0}	$1/7 * t_{CLK} - 0.4$	$1/7 * t_{CLK}$	$1/7 * t_{CLK} + 0.4$	ns
	1st data position	t_{RP1}	-0.4	0	+0.4	
	2nd data position	t_{RP2}	$6/7 * t_{CLK} - 0.4$	$6/7 * t_{CLK}$	$6/7 * t_{CLK} + 0.4$	
	3rd data position	t_{RP3}	$5/7 * t_{CLK} - 0.4$	$5/7 * t_{CLK}$	$5/7 * t_{CLK} + 0.4$	
	4th data position	t_{RP4}	$4/7 * t_{CLK} - 0.4$	$4/7 * t_{CLK}$	$4/7 * t_{CLK} + 0.4$	
	5th data position	t_{RP5}	$3/7 * t_{CLK} - 0.4$	$3/7 * t_{CLK}$	$3/7 * t_{CLK} + 0.4$	
	6th data position	t_{RP6}	$2/7 * t_{CLK} - 0.4$	$2/7 * t_{CLK}$	$2/7 * t_{CLK} + 0.4$	

8.7 DATA INPUT for DISPLAY COLOR

1) 8 Bit Mode

Input		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
color		MSB				LSB				MSB				LSB				MSB				LSB			
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (0)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (0)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (61)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (1)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (0)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (61)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Green (253)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (2540)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
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	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	0
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

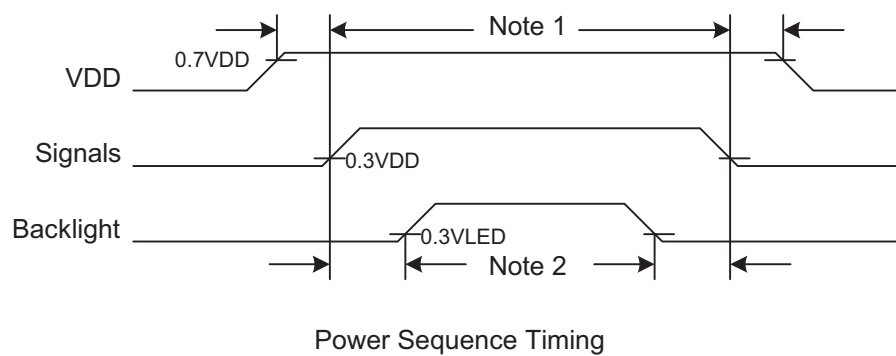
Note 1: Definition of gray scale :

Color(n)----Number in parenthesis indicates gray scale level.

Larger number corresponds to brighter level.

Note 2: Data signal : 1:High, 0 : Low

8.8 POWER SEQUENCE

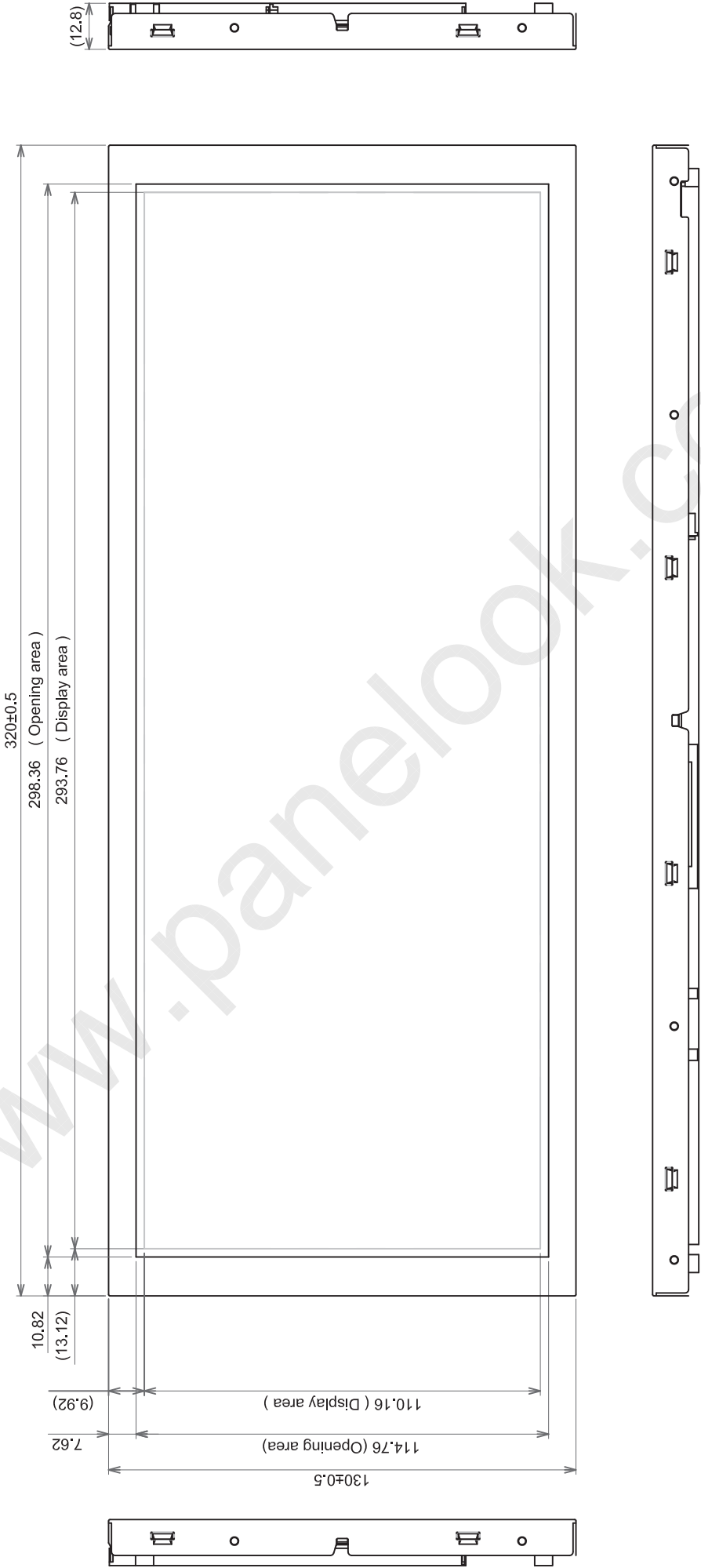


Note 1: In order to avoid any damages, VDD has to be applied before all other signals. The opposite is true for power off where VDD has to be remained on until all other signals have been switch off. The recommended time period is 1 second. Hot plugging might cause display damage due to incorrect power sequence, please pay attention on interface connecting before power on.

Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the signals are removed.

9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



Note1. General tolerance ± 0.5

Scale : NTS
Unit : mm

Note1. General tolerance ± 0.5